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APPLICATION NO	. FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/769,146	01/29/2004	Junichiro Watanabe	2102475-991320	8510	
26379	7590 09/20/	006	EXAM	EXAMINER	
	ER RUDNICK GRA	NGUYEN, TUAN H			
	/ERSITY AVENUE ALTO, CA 94303-22	18	ART UNIT	PAPER NUMBER	
	<b>,</b>		2813		
			DATE MAILED: 09/20/200	6	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Ap	pplicant(s)	_///
	10/769,146	l w	WATANABE, JUNICHIRO	
Office Action Summary	Examiner	Ar	t Unit	
	Tuan H. Nguyen	1	l l	
The MAILING DATE of this communication Period for Reply	appears on the cove	r sheet with the corre	espondence address	
A SHORTENED STATUTORY PERIOD FOR REWHICHEVER IS LONGER, FROM THE MAILING  Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication  If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by some any reply received by the Office later than three months after the rearned patent term adjustment. See 37 CFR 1.704(b).	G DATE OF THIS CO R 1.136(a). In no event, how n. eriod will apply and will expire tatute, cause the application t	DMMUNICATION.  ever, may a reply be timely fi  SIX (6) MONTHS from the map become ABANDONED (3)	led nailing date of this communication.	
Status				
1) Responsive to communication(s) filed on 1	11 July 2006			
	This action is non-fin	al.		
3) Since this application is in condition for all			cution as to the merits is	
closed in accordance with the practice und				
Disposition of Claims				
4)⊠ Claim(s) <u>2-5,29 and 30</u> is/are pending in th	ne application			
4a) Of the above claim(s) is/are with		ation		
5) Claim(s) is/are allowed.				
6)⊠ Claim(s) <u>2-5,29 and 30</u> is/are rejected.				
7) Claim(s) is/are objected to.				
8) Claim(s) are subject to restriction are	nd/or election require	ment.		
Application Papers				
9)☐ The specification is objected to by the Exar	niner			
10) The drawing(s) filed on is/are: a)		ected to by the Exa	miner	
Applicant may not request that any objection to				
Replacement drawing sheet(s) including the co				
11) The oath or declaration is objected to by the				
Priority under 35 U.S.C. § 119				
12)⊠ Acknowledgment is made of a claim for fore	eian priority undor 35	U.S.C. S. 140(a) (d)	or (f)	
a)⊠ All b)□ Some * c)□ None of:	eigh phonty under 55	0.3.C. 9 119(a)-(d)	Of (1).	
1.⊠ Certified copies of the priority docum	nents have been rece	ived		
2. Certified copies of the priority docum			Νo	
3. Copies of the certified copies of the				
application from the International Bu			· · · · · · · · · · · · · · · · · · ·	
* See the attached detailed Office action for a	·	7 7 7		
Attachment(s)				
1) Notice of References Cited (PTO-892)		Interview Summary (PTC	D-413)	
<ol> <li>Notice of Draftsperson's Patent Drawing Review (PTO-948</li> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SE Paper No(s)/Mail Date</li> </ol>	) 3/08) 5) 🔲	Paper No(s)/Mail Date Notice of Informal Patent Other:	·	
S. Patent and Trademark Office TOL-326 (Rev. 7-05) Office	ce Action Summary	Part of	Paper No./Mail Date 20060917	
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### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 29, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Boerstler et al. (US 2005/0088794).

Boerstler et al., fig. 5 discloses the claimed semiconductor integrated circuit including an internal circuit (protected elements such as processors 502) having first and second I/O external terminals 501 connected to the internal circuit, first and second fuse elements 504, each having first and second terminals, the first terminals of the first and second fuse elements being respectively connected to the first and second external terminals 501, and discharge line 508 or 511 connected to the second terminals of the first and second fuse elements and serving as an electrostatic discharge current path.

With respect to claim 5, see paragraph [0001].

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

**Art Unit: 2813** 

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boerstler et al..

Boerstler et al. in disclosing the claimed semiconductor integrated circuit as explained above fails to teach the resistance value, maximum energy level or breakdown current of the first and second fuses before they break to protect the circuit. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the basic formula to figure out the minimum resistance value, energy or current so that it would break at the voltage below the breakdown voltage of the device that is protected.

With respect to claim 30, it has been obvious to one having ordinary skill in the art to have used a plurality of MOS transistors for forming an integrated circuit in the semiconductor art, and I/O terminals are connected to gates of the MOS transistors for controlling the currents between sources and drains.

#### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

#### Response to Arguments

Applicant's arguments filed 7/11/06 have been fully considered but they are not persuasive. Contrary to the Applicant's argument in his Remarks, page 4, last two lines of fourth paragraph that "Boerstler does not discloses an integrated circuit whose power supply terminal is connected to its internal circuit". First of all, the limitation is not recited in the instant claims therefore it is irrelevant; secondly, assuming that there is no power supply terminal is connected to its integrated circuit, how could the integrated circuit be able to operate without the power supply. Note that figure 5 shows an integrated circuit with multiple I/O pads connected to an internal circuit having a plurality of protected elements 502, and the internal circuit is connected to the same common voltage line 516. One end of the fuse 504 is connected to the I/O pad 501, the other end of the fuse 504 is directly connected to the discharge line through diodes 505 or 506 to Vdd 508 or ground 511 respectively and served as an electrostatic discharge current path. The

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discharge line as claimed does not preclude the use of diodes 505 or 506 as disclosed

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by Boerstler.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-

1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen Primary Examiner

Juan H. Nguyen

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